

Substitute for Form 1449/PTO

INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

Application Number	09/752,541
Filing Date	12-29-00
First Named Inventor:	Boyd, et al.
Art Unit	2124
Examiner Name	Tuan A. Vu
Attorney Docket Number	004363.P001

Sheet

of

6

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
MJS ↓ JAT		US-	5,973,524	10/26/1999	Martin	
		US-	6,269,277 B1	07/31/2001	Hershenson	
		US-	4,827,428	05/02/1989	Dunlop, et al.	
		US-	6,381,563 B1	04/30/2002	O'Riordan, et al.	
		US-	6,532,569 B1	03/11/2003	Christen, et al.	
		US-	6,577,992 B1	06/10/2003	Tcherniaev, et al.	
		US-	6,425,111 B1	07/23/2002	del Mar Hershenson	
		US-	6,311,145 B1	10/30/2001	Hershenson	
		US-	6,581,188	06/17/2003	Hosomi, et al.	
		US-	6,311,315	10/30/2001	Tamaki	
		US-	6,002,860	12/14/1999	Voinigescu, et al.	
		US-	5,754,826	05/19/1998	Gamal, et al.	
		US-	5,633,807	05/27/1997	Fishburn, et al.	
		US-	5,055,716	10/8/1991	El Gamel	
		US-	5,289,021	02/22/1994	El Gamel	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				
MJS		GB	2 131 228 A	6/13/1984	RCA Corporation		

Examiner
Signature

Tuan A. Vu

Date Considered

09-09-05

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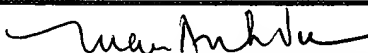
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Based on Form PTO/SB/08B (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) JUN 27 2005 U.S. PATENT & TRADEMARK OFFICE		Application Number	09/752,541
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
AT		MEDIERO, F., et al., "A Vertically Integrated Tool For Automated Design Of Sigma Delta Modulators", IEEE Journal of Solid-State Circuits, Vol. 30., No. 7, July 1, 1995, pp. 762-767.	
AT		VON KAENEL, V., et al., "A 320MHz, 1.5mW at 1.36V CMOS PLL For Microprocessor Clock Generation", IEEE Solid-State Circuits Conference, November 9, 1996, Digest of Technical Papers, 42nd ISSCC96/ SESSION 8 / DIGITAL CLOCKS AND LATCHES / PAPER FA 8.2.	
AT		CHAN, et al., "Analysis of Linear Networks and Systems," Addison-Wesley Publishing Company, 1972, pp. 23-25 and 46-57.	
AT		YOUNG, et al., "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessor", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pp. 1599-1607.	
AT		NOVOF, et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ± 50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30., No. 11, November 1995, pps. 1259-1266.	
AT		MOHAN, et al., "Simple Accurate Expressions for Planar Spiral Inductances", IEEE Journal of Solid-State Circuits, Vol. 34, No. 10, October 1999, pp. 1419-1424.	
AT		HERSHENSON, "CMOS Analog Circuit Design Via Geometric Programming", A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University, November 1999, 241 pages.	
AT		HERSHENSON, M., et al., "Optimization of Inductor Circuits via Geometric Programming", pp. 994-998, Design Automation Conference, June 21, 1999, Proceedings.	
AT		HERSHENSON, M., et al., "Automated Design of Folded-Cascode Op-Amps with Sensitivity Analysis", pp. 121-124, Electronics, Circuits and Systems, IEEE International Conference on LISBOA, September 7-10, 1998.	
NC		GIELEN, G., et al., "An Analogue Module Generator For Mixed Analogue/Digital ASIC Design", International Journal of Circuit Theory and Applications, Vol. 23, pp. 269-283, 1995.	NC
AT		KORTANEK, K.O., et al., "An Infeasible Interior-Point Algorithm For Solving Primal And Dual Geometric Programs," pp., 155-181, Mathematical Programming Society, Inc., 76:155-181, January 1, 1995.	

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AT		HERSHENSON, M., et al., "GPCAD: A Tool for CMOS Op-Amp Synthesis" 8 pages, Proceedings of the IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 296-303, November 1998.	
AT		HERSHENSON, M., et al., "Posynomial models for MOSFETs" 9 pages, July 7, 1998.	
AT		CHANG, H, et al., "A Top-Down, Constraint-Driven Design Methodology for Analog Integrated Circuits" 6 pages, IEEE 1992 Custom Integrated Circuits Conference.	
AT		CHAVEZ, J., et al, "Analog Design Optimization: A Case Study" 3 pages, IEEE, January 1993.	
AT		GEILEN, G., et al., "Analog Circuit Design Optimization Based on Symbolic Simulation and Simulated Annealing", pp. 707-713, IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, June 1990.	
AT		FISHBURN, J, et al., "TILOS: A Posynomial Programming Approach to Transistor Sizing" pp. 326-328, IEEE, 1985.	
AT		MAULIK, P., et al., "Integer Programming Based on Topology Selection of Cell-Level Analog Circuits", 12 pages, IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 14, No. 4, April 1995.	
AT		SWINGS, K., et al., "An Intelligent Analog IC Design System Based On Manipulation Of Design Equations" pp. 8.6.1- 8.6.4, IEEE 1990, Custom Integrated Circuits Conference.	
AT		NESTEROV, Y., et al., "Interior-Point Polynomial algorithms in Convex Programming" 8 pgs., 1994, Society for Industrial and Applied mathematics.	
AT		YANG, H.Z., et al., "Simulated Annealing Algorithm with Multi-Molecule: an Approach to Analog Synthesis" pp. 571-575, IEEE, 1996.	
AT		WONG, D.F., et al., "Simulated Annealing For VLSI Design" 6 pages, 1998, Kulwer Academic Publishers.	

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NAT		MAULIK, P., et al., "Sizing of Cell-Level Analog Circuits Using Constrained Optimization Techniques" pp. 233-241, IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993.			
NAT		OCHOTTA, E, et al., "Synthesis of High -Performance Analog Circuits in ASTRX/OBLS" pp. 273-295, IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, Vol. 15, No. 3, March 1996.			
NAT		WRIGHT, S., "Primal-Dual Interior-Point Methods" pp. 1-3, http://www.siam.org/books/wright , Printed August 19, 1998.			
NAT		SHYU, J., et al., "Optimization-Based Transistor Sizing" pp. 400-408, IEEE Journal of Solid-State Circuits, Vol. 23, No. 2, April 1998.			
NAT		WRIGHT, S., "Primal-Dual Interior-Point Methods" 14 pages, 1997, Society for Industrial and Applied Mathematics.			
NAT		VAN LAARHOVEN, P.J.M., et al., "Simulated Annealing: Theory and Applications" 26 pages, 1987, Kulwer Academic Publishers.			
NAT		HERSHENSON, M., et al., "CMOS Operational Amplifier Design and Optimization via Geometric Programming" pp. 1-4, Analog Integrated Circuits, Stanford University.			
NAT		AGUIRRE, M.A., et al., "Analog Design Optimization by means of a Tabu Search Approach" pp. 375-378.			
NAT		MEDEIRO, F., et al., "A Statistical Optimization-Based Approach for Automated Sizing of Analog Cells", pp. 594-597, Dept. of Analog Circuit Design.			
NAT		SPATNEKAR, S., "Wire Sizing as a Convex Optimization Problem: Exploring the Area-Delay Tradeoff" 27 pages, Dept. of Electrical and Computer Engineering.			
NAT		SU, H., et al., "Statistical Constrained Optimization of Analog MOS Circuits Using Empirical Performance Models" pp. 133-136.			

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AT		VASSILIOU, I., et al, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology" 6 pages.		
AT		SAPATNEKAR, S, et al., "An Exact Solution to the Transistor Sizing Problem for CMOS Circuits Using Convex Optimization" 35 pages.		
AT		BOWMAN, R., "An Imaging Model For Analog Macrocell Layout Generation", IEEE International Symposium On Circuits And Systems, Vol. 2, 8 May 1989, pp. 1127-1130, XP010085007.		
AT		HUNTER, A., et al., "Combining Advanced Process Technology and Design for Systems Level Integration", IEEE Proceedings, pages 245-250, First International Symposium On Quality Electronic Design, March 20, 2000		

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